In_2O_3 Nanocrystal Memory with Barrier Engineered Tunnel Layer

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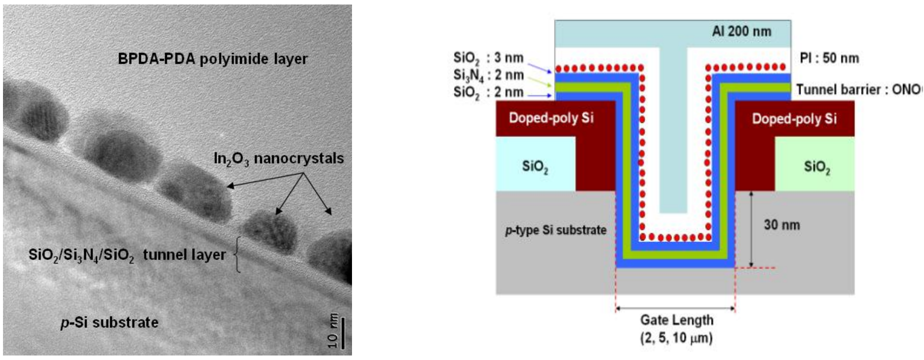
The tunnel oxide thickness has a difficult problem to scale down for the improvement of endurance and charge retention properties of the non-volatile memory. Also, the nanocrystal nonvolatile memory applications require the tunnel barrier to have relatively low applied voltage for long retention time and fast speed [1]. In this study, the In_2O_3 nanocrystals memories with barrier engineered tunnel layer were fabricated on *p*-type Si substrate. The structure and thickness of barrier engineered tunnel layer were $SiO_2/Si_3N_4/SiO_2$ (ONO) and 2 nm/ 2 nm/ 3nm, respectively. A 50-nm-thick polyamic acid (PAA) precursor was spin coated on the deposited indium film. This PAA precursor is a biphenyl dianhydride-p-phenylenediamine (BPDA-PDA) type. Then, the samples were cured at 400 ^oC for an hour in a rapid thermal annealing (RTA) system. The deposition of aluminum layer with thickness of 150 nm was followed by using a thermal evaporator, and then the gate electrode was defined by photolithography and etching. Finally, the phosphorus plasma doping at 400 ^oC was carried out for source-drain doping of device [2]. Figure 1(a) shows a cross-sectional TEM image the In_2O_3 nanocrystals with ONO tunnel layer. The size and density of In_2O_3 nanocrystals are about 7 nm and $6x10^{11}$ cm^{-2}, respectively [3]. The cross-sectional schematic diagram of In_2O_3 nanocrystal memory is shown in Fig. 1(b). We will discuss a feasibility of In_2O_3 nanocrystal application for the tunnel barrier engineered nonvolatile memory.



(a) (b)

Figure 1. (a) a cross-sectional TEM image and (b) a schematic diagram of In_2O_3 nanocrystals nonvolatile memory.

References

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